X-544-64-394

NASA TMX-55179

PORTABLE PFM SIMULATOR

DECEMBER 1964

NASA — GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

PORTABLE PFM SIMULATOR

Designers:

Harold Levy
Paul Heffner
Joseph Tinsley

Data Instrumentation Branch
Data Systems Division

September 1964

GODDARD SPACE FLIGHT CENTER
Greenbelt, Maryland

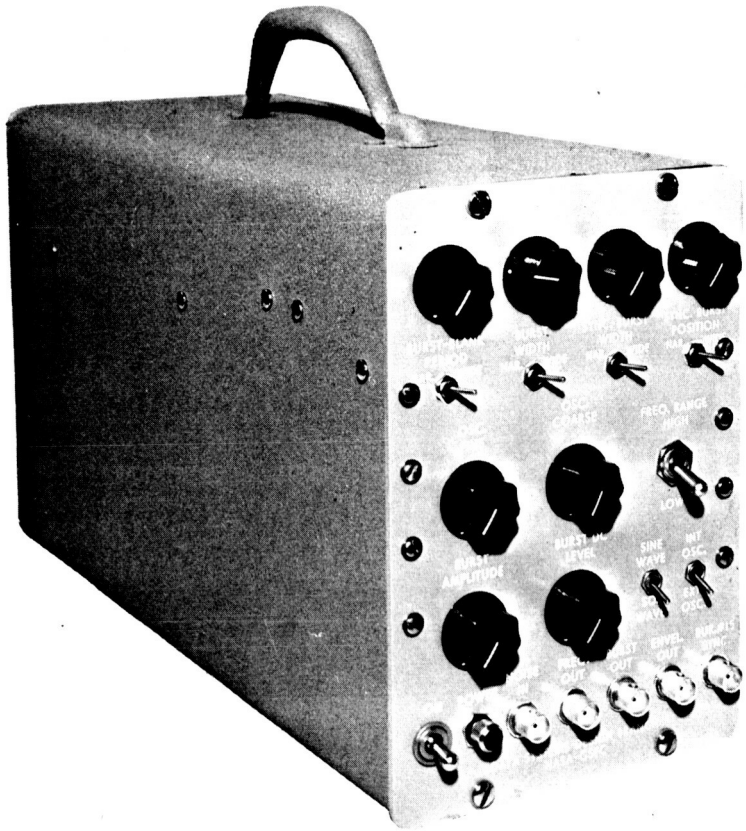
CONTENTS

	Page
INTRODUCTION	1
SPECIFICATIONS	3
OPERATING INSTRUCTIONS	4
DESCRIPTION AND THEORY OF OPERATION	4
CIRCUITS	7
BISTABLE MULTIVIBRATOR (FLIP-FLOP) CIRCUIT	7
RUNDOWN CIRCUIT	14
NAND CIRCUIT	15
SCHMITT TRIGGER AND AMPLIFIER	18
OSCILLATOR CIRCUIT	21
AUTOMATIC VOLTAGE-CONTROLLED (AVC) CIRCUIT	22
OSCILLATOR GATE	25
POWER SUPPLY	25
PERFORMANCE CHECK	25

ILLUSTRATIONS

Figure		Page
Frontispiece—Portable PFM Simulator		vi
1	Typical Module Board	2
2	Simulator Waveforms	5
3	PFM Simulator Logic, Block Diagram	6
4	PFM Simulator, Phase Synchronization Logic Waveforms	8
5	PFM Simulator, Schematic Diagram	9
6	PFM Simulator, Wiring Diagram	11
7	Flip-flop Circuit	13
8	Rundown and Flip-flop, Operating as Multivibrator	15
9	Rundown Circuit	16
10	NAND Circuits	17
11	Schmitt Trigger and Amplifier	19
12	Oscillator, AVC, and Oscillator Gate Circuits	20
13	AVC Loop	23
14	Complete L Pad	23
15	AC-Equivalent L Pad	23
16	Equivalent L Pad Seen by Input Signal	24
17	Diode Characteristic Curve	24
18	Power Supply	26
19	Brown Test Point, Card 3	27

Figure		Page
20	Red Test Point, Card 3	28
21	Red and Brown Test Points, Card 3	28
22	Yellow Test Point, Card 3	29
23	Orange Test Point, Card 3	29
24	Orange and Yellow Test Points, Card 3	30
25	Brown Test Point, Card 2	30
26	Brown Test Point, Card 1	31
27	Sinewave Adjustment	31
28	Square Wave Adjustment	32
29	Typical Waveforms	33
30	Oscilloscope Pattern Showing Correct Adjustment	34
31	SYNC BURST Variation	34



Frontispiece - Portable PFM Simulator

PORTABLE PFM SIMULATOR

INTRODUCTION

The pulse-frequency modulation (PFM) simulator was designed in 1960 as a laboratory instrument to assist in the design and checkout of PFM equipment. Criteria for flexibility, data burst rates, data frequency ranges, etc., were based on previous PFM satellite ranges and expected future ranges.

The unit simulates the synchronous 16-channel frame pulse-frequency-modulated signal with frame-synchronization burst. Burst width, burst frequency, and burst amplitude are available by front panel control. The frame-synchronization burst can be positioned where desired at the beginning of the frame. The unit covers the data burst-rate range of 20 to 250 data bursts per second, and is continuously variable over these limits in just two ranges. The frequency within the data burst may be internally or externally applied; noise may be linearly summed with the signal by applying a noise generator signal to the unit.

The unit, which is fully transistorized, employs functional printed-circuit modules (Figure 1), including the power-supply regulator. All circuits were designed by the Data Instrumentation Development Branch. All outputs from the unit are protected against short circuits to ground.

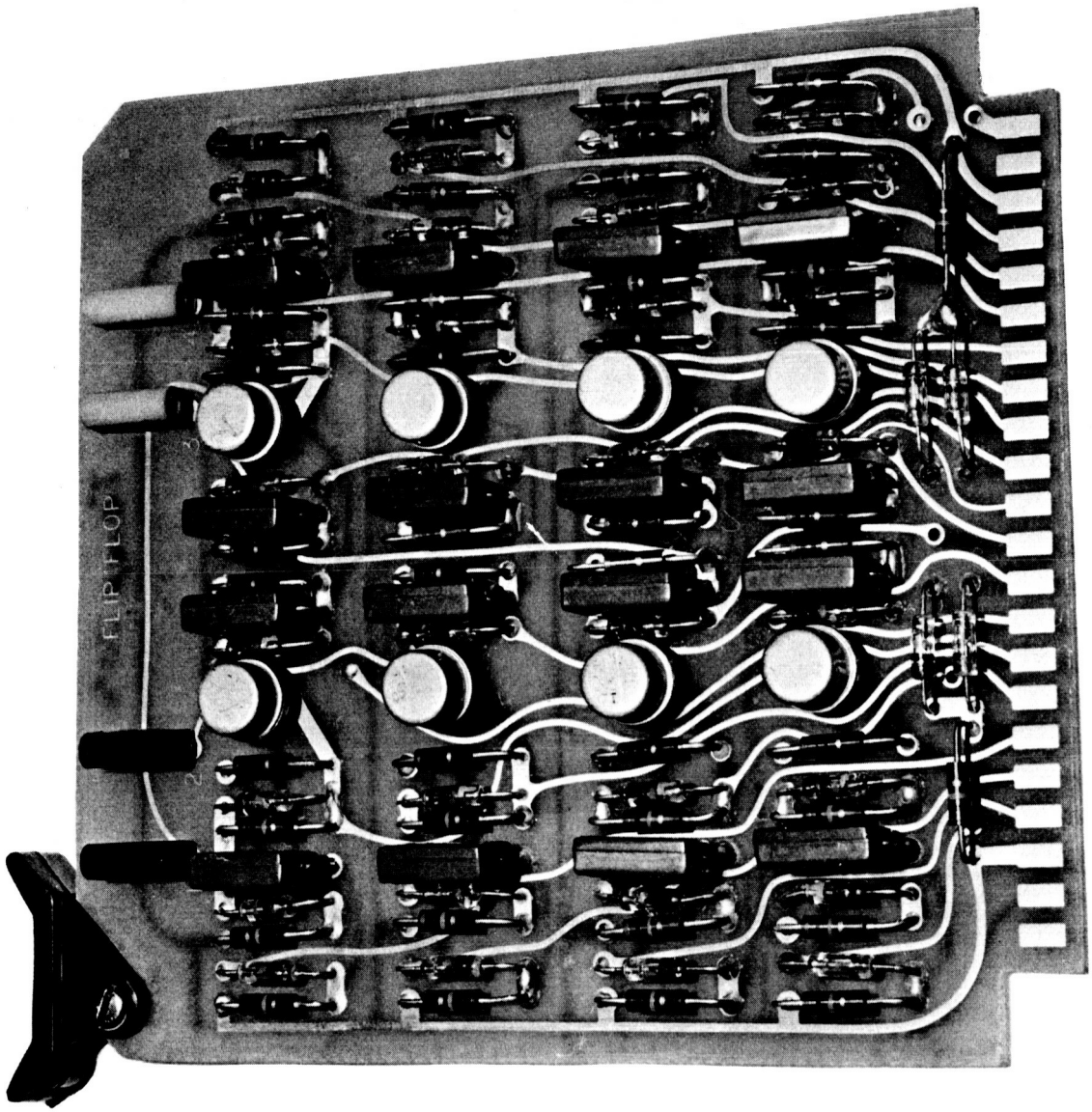


Figure 1 – Typical Module Board

SPECIFICATIONS

Signal:	Synchronous, pulse-frequency modulated, 16-channel frame with a synchronization burst
Channels:	
Number:	Sixteen
Burst frequency:	Internal or external (internal frequency continuously variable in two ranges covering 4.5 to 45 kc)
Burst duration:	Continuously variable, 0.5 to 50 msec in two ranges
Burst amplitude:	Continuously variable, 0 to 4 vpp
Burst dc level:	± 0.5v continuously variable about 0vdc level of signal
Synchronization Burst:	Control to position the sync burst between channel 15 and channel 2
Repetition Rate (simulated sampling rate):	20 cycles/sec to 2 kilocycles/sec continuously variable, 2 ranges
Inputs and Input Impedances:	
Noise input:	6.1 kilohms
Ext. osc. input:	18 kilohms
Outputs and Output Impedances:	
Frequency burst output:	100 ohms
Burst envelope output:	1 kilohms
Comp. envelope output:	100 ohms
Burst #15 sync output:	1 kilohm
Power:	105-120 volts rms 60 watts
Environment Temperature:	0°C to 50°C
Structure:	Portable case
Height	8-1/2 inches
Width	5-3/4 inches
Depth:	17 inches
Controls:	Front panel

OPERATING INSTRUCTIONS

The PFM simulator unit operates on a standard 117-volt line. The BURST DC LEVEL control adjusts the dc level of the frequency burst with respect to the level of the blank for each burst and blank throughout the frame. In essence, this is a bias control to the oscillator AND gate. With large changes in temperature this control must be adjusted. The frequency within the burst must be measured by external means using, for example, an oscilloscope or a frequency counter. An appropriate sequence for operating the unit is:

1. Turn power switch to ON.
2. Throw INT. OSC.-EXT. OSC. switch to mode desired.
3. Synchronize oscilloscope to burst #15 sync output.
4. Turn BURST WIDTH and SYNC BURST WIDTH controls to minimum burst width.
5. Adjust BURST DC LEVEL.
6. Adjust BURST-BLANK controls.
7. Adjust BURST WIDTH controls.
8. Adjust SYNC. BURST WIDTH and SYNC. BURST POSITION controls.
9. Monitoring FREQ output, adjust frequency controls.
10. Throw SINEWAVE-SQ. WAVE switch to signal desired.
11. Adjust BURST AMPLITUDE.

DESCRIPTION AND THEORY OF OPERATION

The principal output of this unit is the 16-burst/blank frame including the synchronizing burst. All bursts consist of a sinewave (or square wave), controllable in two ranges of 5 to 15 kc and 15 to 45 kc. The burst amplitude can be varied from 0 to 4 volts peak-to-peak. The synchronizing burst width and occurrence in time relative to the preceding burst are individually controllable. The burst-blank period and the burst within the burst-blank period are adjustable over two ranges of 0.5 to 4 msec and 4 to 50 msec. The waveform within the burst may be switched to either a sinewave or a square wave. In either case, the waveform swings about the dc level of the blank period (Figure 2). The frequency of the square wave is that of the sinewave oscillator setting. The frequency within the burst may be provided by an external oscillator in order to obtain frequencies not attainable in the given ranges of the internal oscillator. The input for the external oscillator is at the rear of the unit.

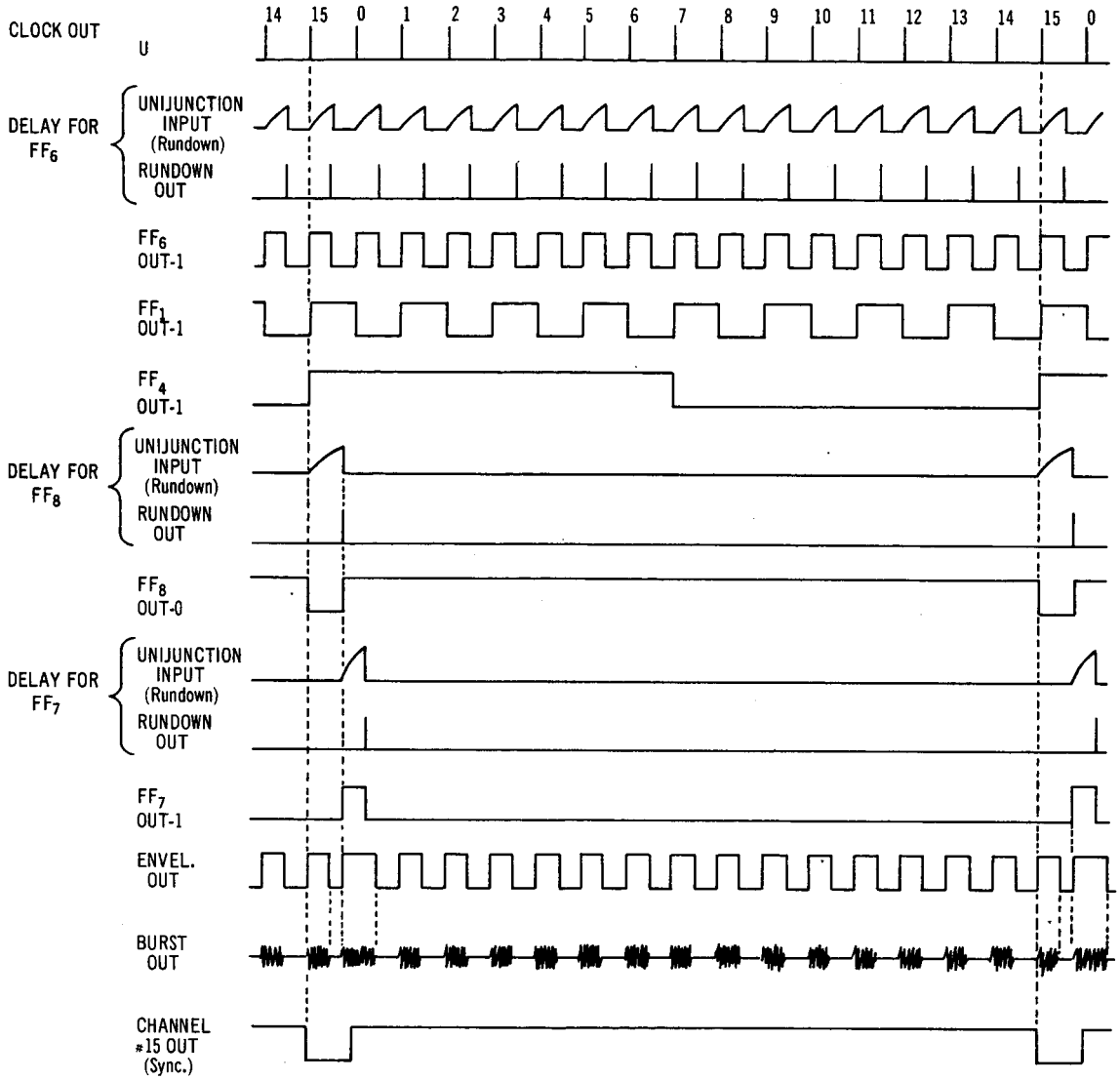


Figure 2 – Simulator Waveforms

The burst-blank period is set by a free-running unijunction rundown circuit which will be referred to as the clock. The clock output is shaped and used to drive both a binary counter and a monostable multivibrator which is a combination of a flip-flop and a unijunction rundown circuit. Referring to Figures 2 and 3, the clock pulse after shaping is seen to trigger flip-flop #6 ON, initiating the rundown which puts out a delayed pulse to trigger the flip-flop OFF. This ON state will gate in the oscillator for the burst (the OFF state will be a blank). The clock also drives flip-flop #1, which is the front end of a binary scale-of-16 counter. After each lapse of 16 burst-blank periods, flip-flop #4 will trigger a

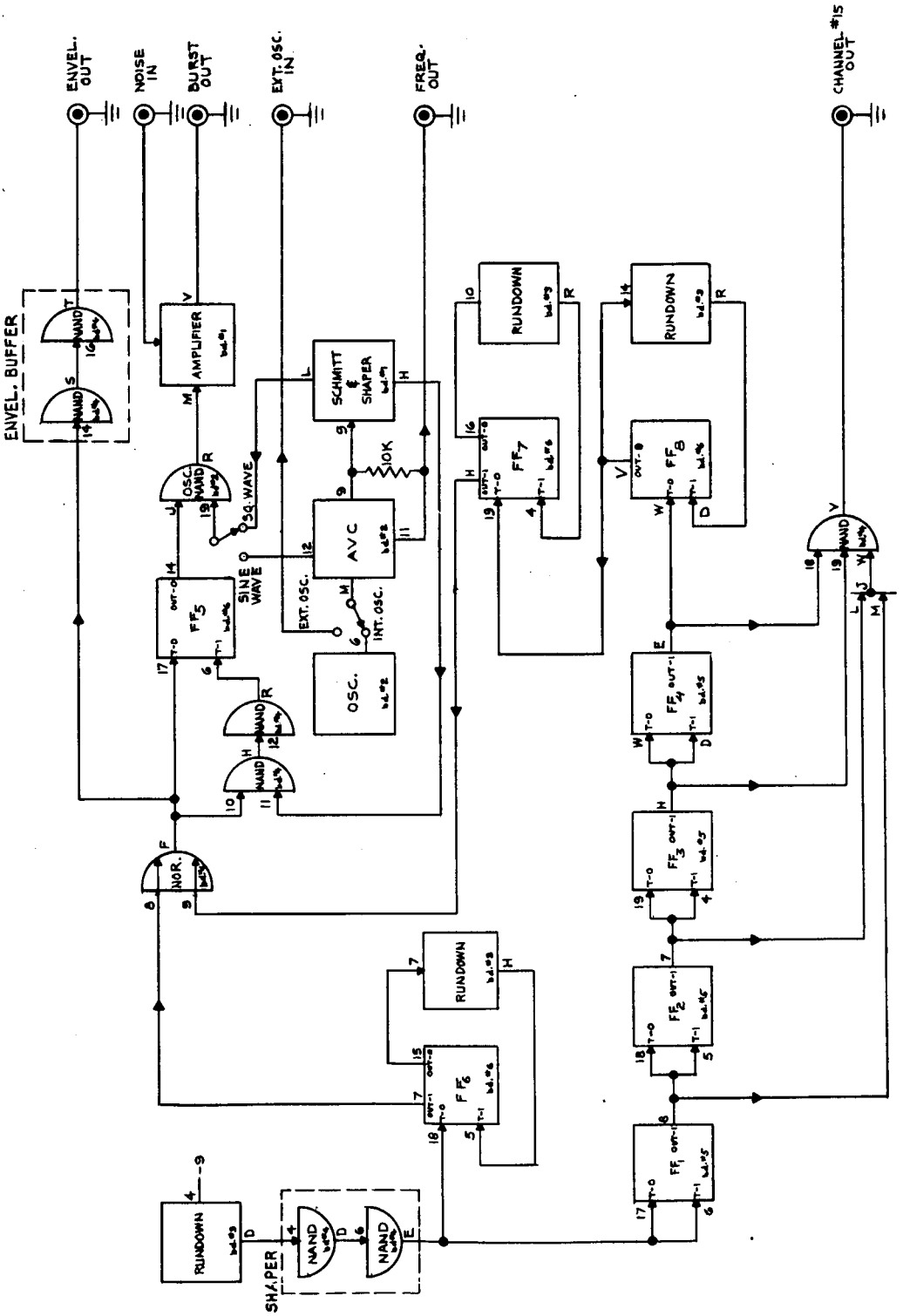


Figure 3 – PFM Simulator Logic, Block Diagram

monostable consisting of flip-flop #8 and its rundown circuit. The delayed rundown pulse triggers flip-flop #8 OFF. The ON state of flip-flop #8 will be the delay setting of the sync burst, referred to as sync burst position. As flip-flop #8 resets after its delay, it will trigger another monostable consisting of flip-flop #7 and its rundown circuit. The ON time of this flip-flop will be the sync burst width.

The burst gates for the sync burst and the following bursts are NOR-functioned so that the combined signal can be passed to the oscillator gate. The signal at this point is also passed through the envelope buffer to the ENV. OUT encoder.

So that the gate time of the burst will not begin at a random phase angle with respect to the incoming continuous sinewave (or square wave) appearing at the oscillator gate, logic is incorporated that will delay the gate until the sinewave (or square wave) passes through the dc level of the signal (Figure 4). This is done by triggering a Schmitt trigger at a dc level commensurate with the dc level of the incoming sinewave. The output of this Schmitt, after shaping, is AND-functioned with the output of the NOR to reset flip-flop #5. The set output (out-0) of this flip-flop at the -9 volt level will gate the OSC.-AND; but this output will not drop to the -9 volt level until the reset input (T-1) receives a positive-going pulse. Inspection of the wave forms in Figure 4 shows that this positive-going reset can occur only at the turn-on time of the Schmitt which was preset to trigger at the level mentioned above. In the square wave mode, a burst will always begin with a full square wave; similarly, in the sinewave mode, a burst will always begin with a full sinewave (the output is shifted by 180 degrees).

The gated sinewave (or square wave) is amplified and ac-coupled to the BURST OUT encoder. A noise signal is applied and algebraically added to the PFM signal at the base of the output emitter-follower. The PFM-signal-amplitude control precedes this stage so that the signal may be reduced within the noise signal. Figures 5 and 6 are the complete schematic and wiring diagrams.

CIRCUITS

BISTABLE MULTIVIBRATOR (FLIP-FLOP) CIRCUIT

The flip-flop circuit (Figure 7) is a JK Eccles-Jordan binary circuit. The reset (j) and set (k) inputs are ac-coupled. By common connection of both the reset and set inputs, the circuit becomes a binary counter. A positive step

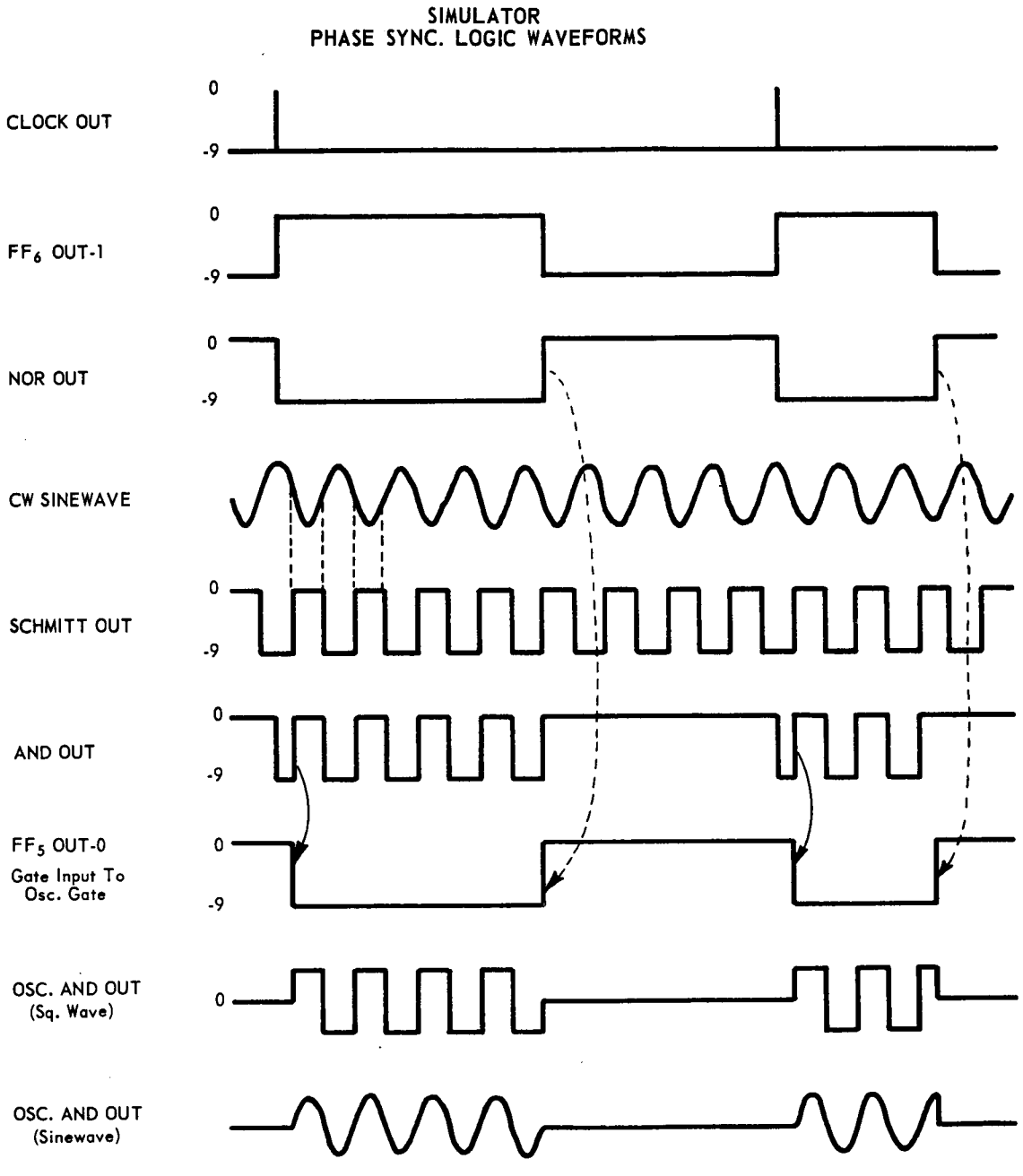


Figure 4 – PFM Simulator, Phase Synchronization Logic Waveforms

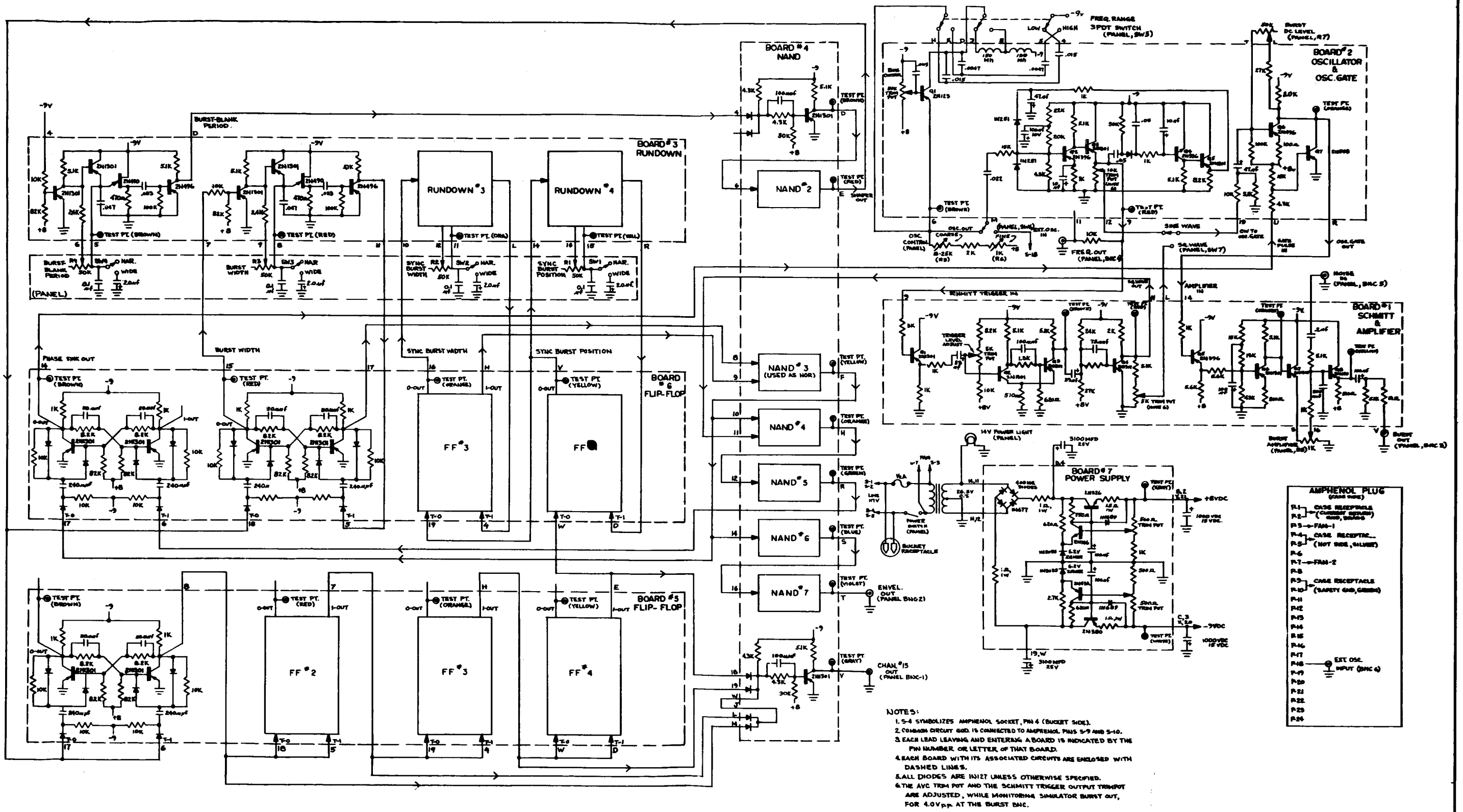
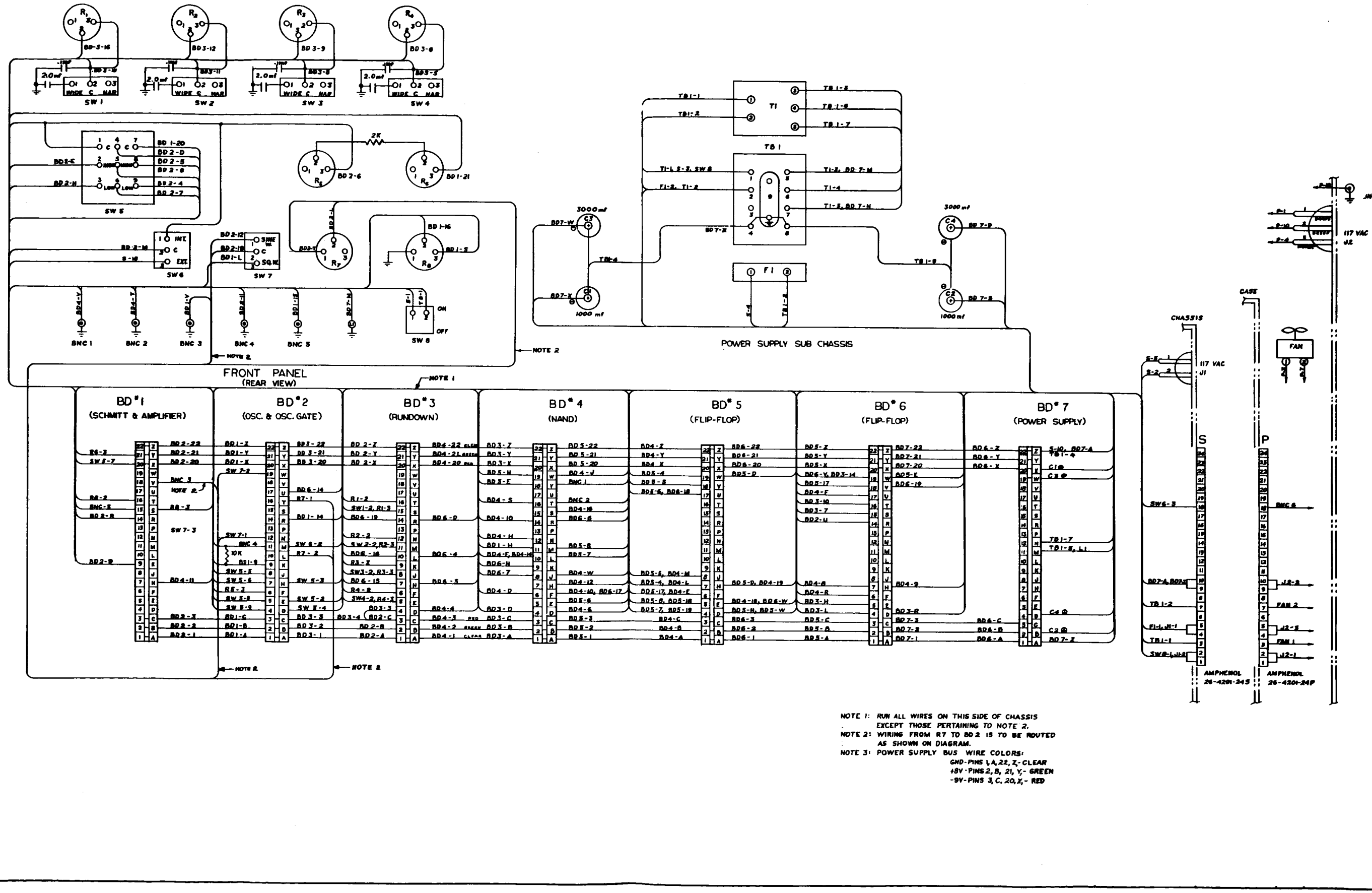
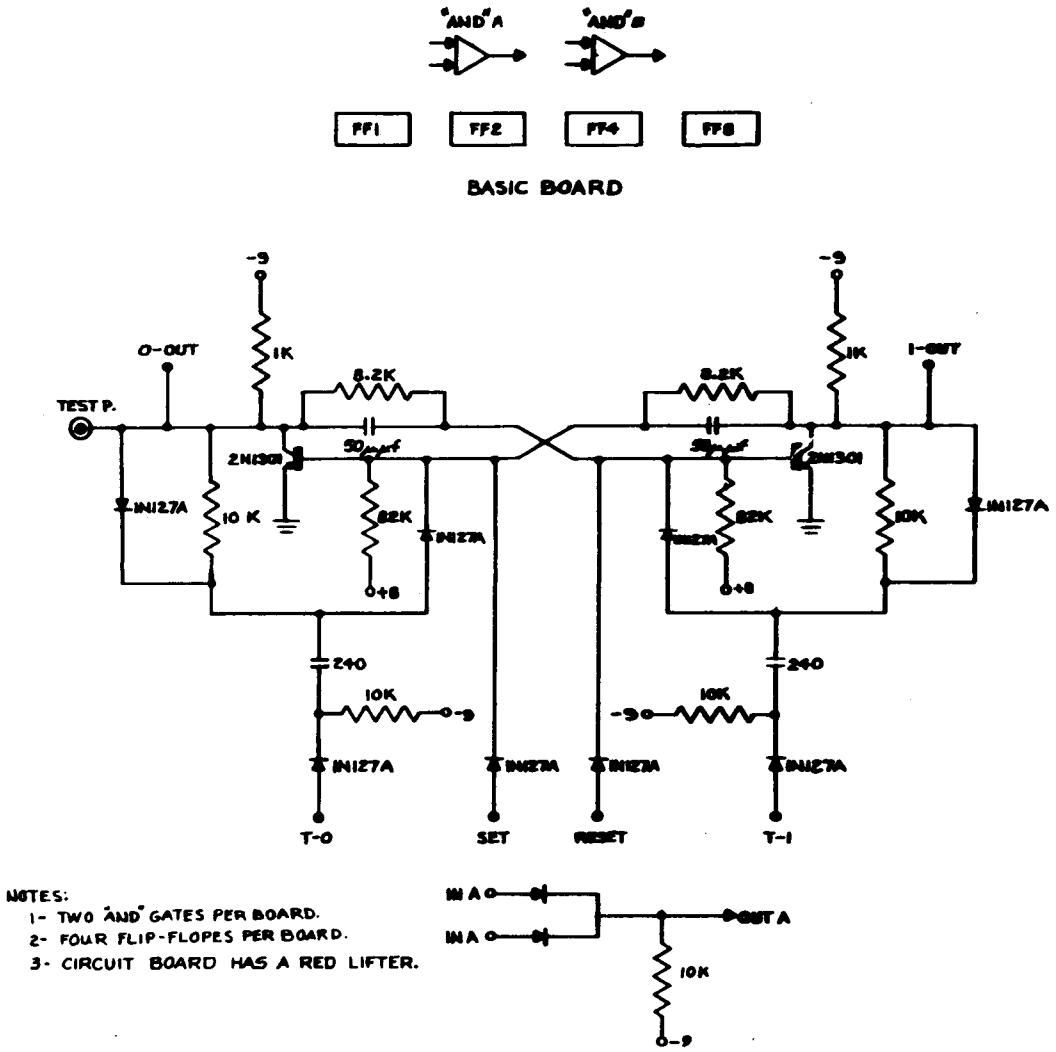


Figure 5 – PFM Simulator, Schematic Diagram



NOTE 1: RUN ALL WIRES ON THIS SIDE OF CHASSIS EXCEPT THOSE PERTAINING TO NOTE 2.
NOTE 2: WIRING FROM R7 TO BD 2 IS TO BE ROUTED AS SHOWN ON DIAGRAM.
NOTE 3: POWER SUPPLY BUS WIRE COLORS:
GND - PINS 1, A, 22, Z, - CLEAR
+8V - PINS 2, B, 21, Y, - GREEN
-9V - PINS 3, C, 20, X, - RED

Figure 6 – PFM Simulator, Wiring Diagram

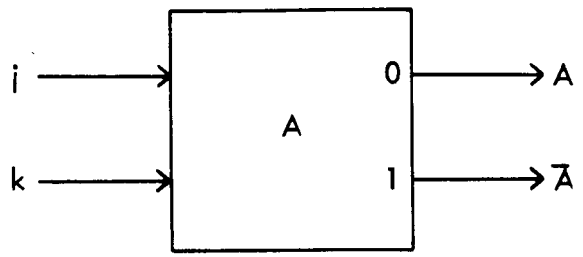


PIN CONNECTIONS

FRONT		BACK	
GND	1	A	GND
+8	2	B	+8
-9	3	C	-9
T1-9	4	D	T1-8
T1-2	5	E	OUT 1-4
T1-1	6	F	OUT AND A
OUT 1-2	7	H	OUT 1-3
OUT 1-1	8	J	RESET-4
RESET-1	9	K	AND A
RESET-2	10	L	AND A
SET-4	11	M	RESET 3
SET-3	12	N	AND B
SET-2	13	P	AND B
OUT 0-1	14	R	SET 4
OUT 0-2	15	S	
OUT 0-3	16	T	
T0-1	17	U	OUT AND B
T0-2	18	V	OUT-0-4
T0-3	19	W	T0-4
-9	20	X	-9
+8	21	Y	+8
GND	22	Z	GND

Figure 7 – Flip-flop Circuit

voltage on the inputs constitute true inputs. The logical function performed by this circuit is shown below:



$$A(\tau) = \bar{k}A + j\bar{A}$$

$$\bar{A}(\tau) = kA + \bar{j}\bar{A}$$

A set input and a reset input are included in the circuit. To employ these inputs a differentiated step voltage is applied.

Four flip-flop circuits and two passive AND gates are on each flip-flop board. The AND gates may be used to implement the four flip-flops as a decimal counter.

RUNDOWN CIRCUIT

The rundown circuit is a circuit which, when used with a flip-flop as shown below, constitutes a wide-range, continuously variable, high-duty cycle monostable multivibrator.

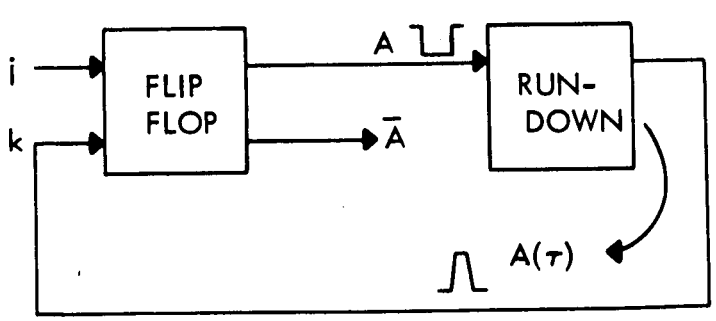


Figure 8 shows the timing relationship of the rundown and flip-flop.

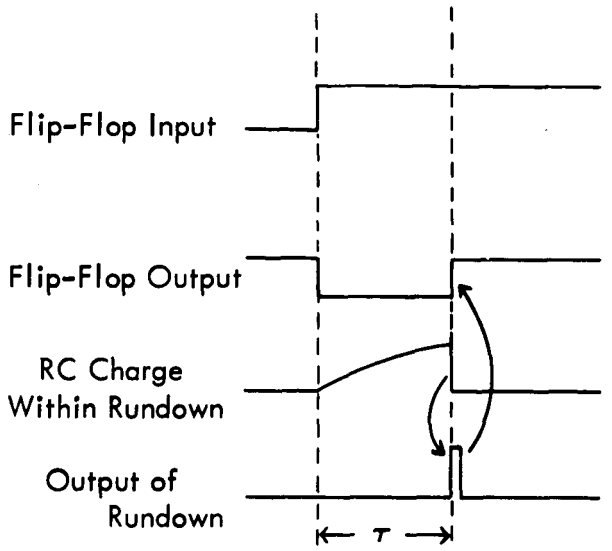


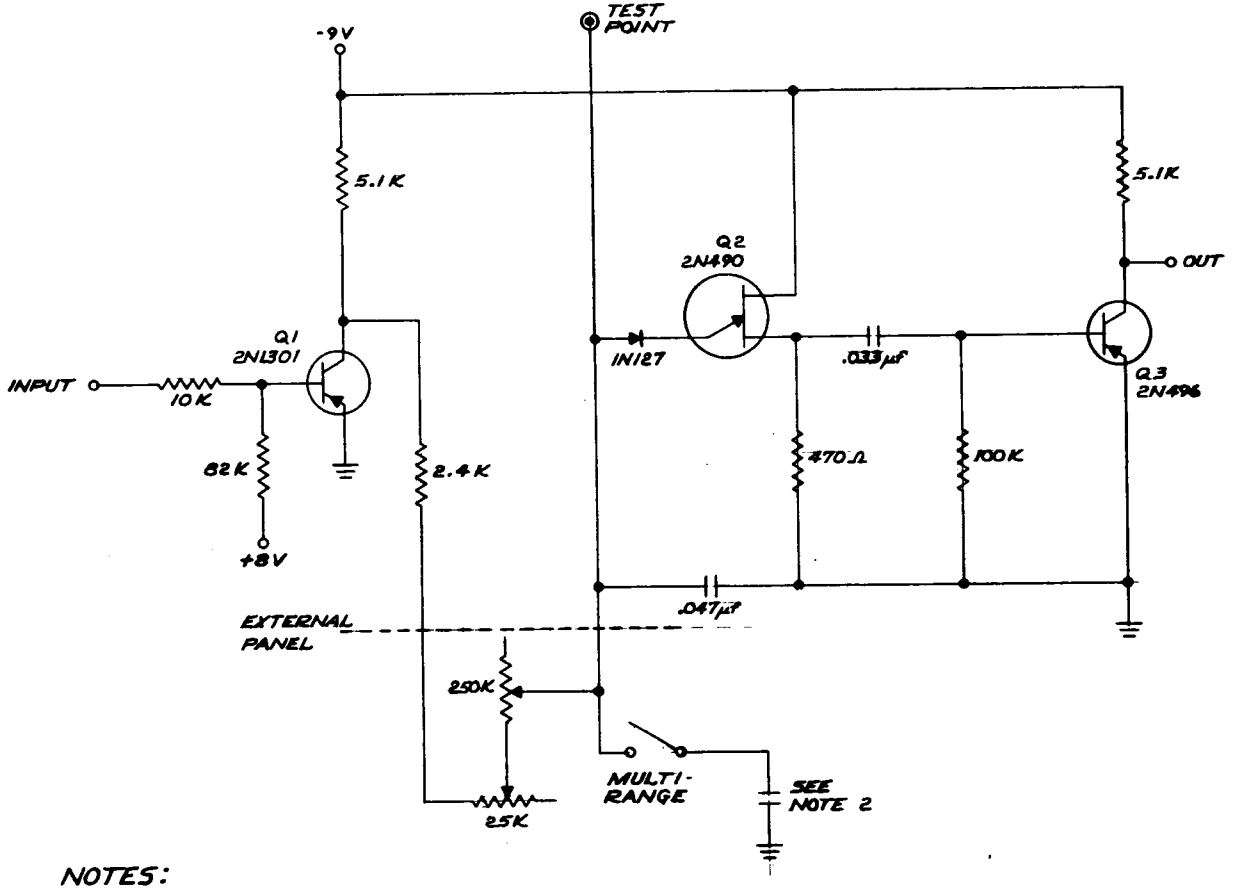
Figure 8 – Rundown and Flip-flop, Operating as Multivibrator

When the input to the rundown circuit steps negatively from ground to -9v, Q_1 saturates and C begins to charge toward ground through the 2.4k resistor and the external front panel potentiometer. When the potential on C reaches the threshold* of the unijunction, it will break into conduction and discharge C to nearly -9v where the unijunction then presents an open circuit to C. The result of the fast discharge of C through the unijunction Q_3 is a negative pulse at B_2 of Q_3, which is coupled to Q_4. This input to Q_4 provides at its output a positive pulse which, as shown in Figure 10, is coupled back to the flip-flop, returning the flip-flop to its original state. This returns the input to the rundown to ground, and turns on Q_2, a clamping transistor, which clamps C to -9v until a new input arrives at Q_1. The delay time (τ) of the circuit is a function of the setting of the front panel potentiometer and the choice of C. There are five rundown circuits on each board. (See Figure 9).

NAND CIRCUIT

The NAND circuit (Figure 10) is a DCTL circuit which (to function as a NAND) requires that all inputs be negative, and (to function as a NOR) requires

*The threshold voltage of a unijunction is defined as $\eta V_{B_1B_2}$ where η is the intrinsic stand-off ratio ($\eta \doteq 0.6$) and $V_{B_1B_2}$ is the voltage impressed across the unijunction.



PIN CONNECTIONS

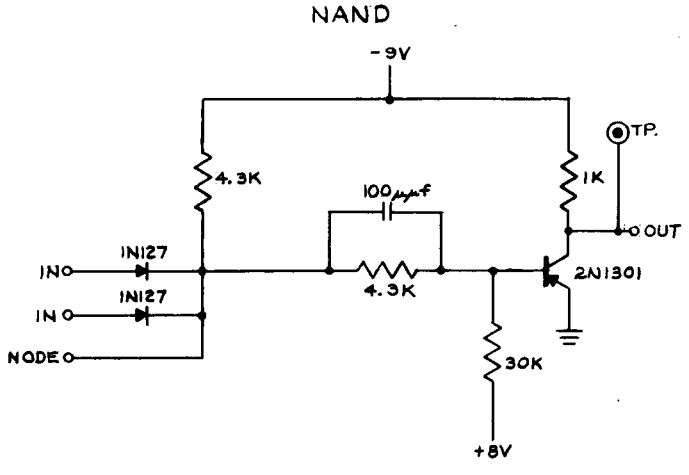
	FRONT	BACK	
GND	1	A	GND
+8V	2	B	+8V
-9V	3	C	-9V
IN-1	4	D	OUT-1
B-1 (POT)	5	E	
A-1 (POT)	6	F	
IN-2	7	H	OUT-2
B-2 (POT)	8	J	
A-2 (POT)	9	K	
IN-3	10	L	OUT-3
B-3 (POT)	11	M	
A-3 (POT)	12	N	
	13	P	
IN-4	14	R	OUT-4
B-4 (POT)	15	S	
A-4 (POT)	16	T	
IN-5	17	U	OUT-5
B-5 (POT)	18	V	
A-5 (POT)	19	W	
-9V	20	X	-9V
+8V	21	Y	+8V
GND	22	Z	GND

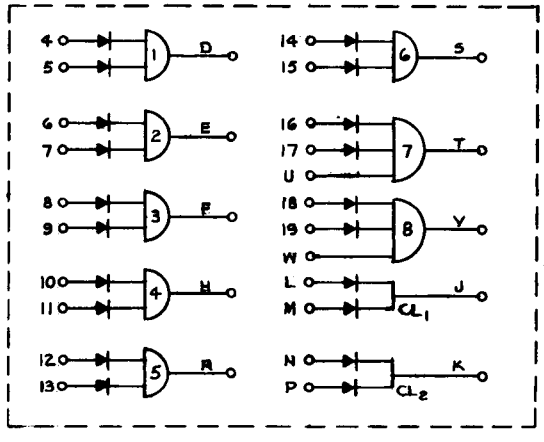
NOTES:

1. FIVE CIRCUITS PER BOARD.
2. DETERMINES RANGE.

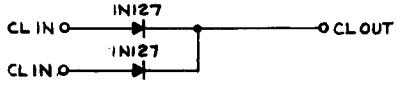
MULTI-RANGE	POT.	CAP.
.5-4 MS	50K	0.1μf
4-50 MS	50K	2.0μf

Figure 9 – Rundown Circuit





CLUSTER



NOTES:

1. CIRCUIT BOARD HAS A YELLOW LIFTER.

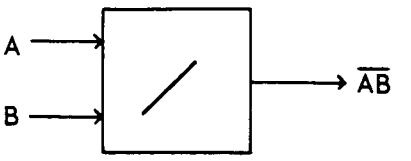
PIN CONNECTIONS

FRONT		BACK
GND	1	A GND
+8	2	B +8
-9	3	C -9
IN1	4	D OUT 1
IN1	5	E OUT 2
IN2	6	F OUT 3
IN2	7	H OUT 4
IN3	8	J CL#1-OUT
IN3	9	K CL#2-OUT
IN4	10	L CL#1-IN
IN4	11	M CL#1-IN
IN5	12	N CL#2-IN
IN5	13	P CL#2-IN
IN6	14	R OUT 5
IN6	15	S OUT 6
IN7	16	T OUT 7
IN7	17	U NODE 7
IN8	18	V OUT 8
IN8	19	W NODE 8
-9	20	X -9
+8	21	Y +8
GND	22	Z GND

Figure 10 – NAND Circuits

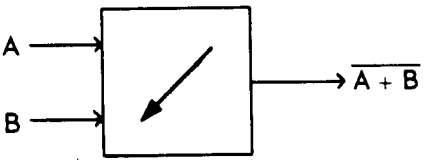
that any one of the inputs be at ground. Logical functions implemented by this circuit are shown below:

(1) As a NAND (for negative logic):



Here the circuit implements the Sheffer stroke function.

(2) As a NOR (for positive logic):



Here, the circuit implements the Peirce function.

Better than 1-volt noise immunity is provided when the input is at ground level. Eight NAND circuits are on each card: Six of the circuits are restricted to a maximum of two inputs, and two circuits are expandable for greater fan-in ability by having a node to which extra input diodes may be connected. Two diode clusters are available with which fan-in may be extended.

SCHMITT TRIGGER AND AMPLIFIER

Figure 11 is a diagram of two separate circuits, a Schmitt trigger and an amplifier.

The Schmitt trigger is a conventional type with a trimpot to adjust the threshold. An input emitter-follower Q1 serves to increase the input impedance and isolate the effect of the threshold adjustment. The common emitter-resistor prevents the Schmitt's Q2 and Q3 output from going to ground. The shaper Q4 is a saturating stage ensuring a complete swing from ground to -9v

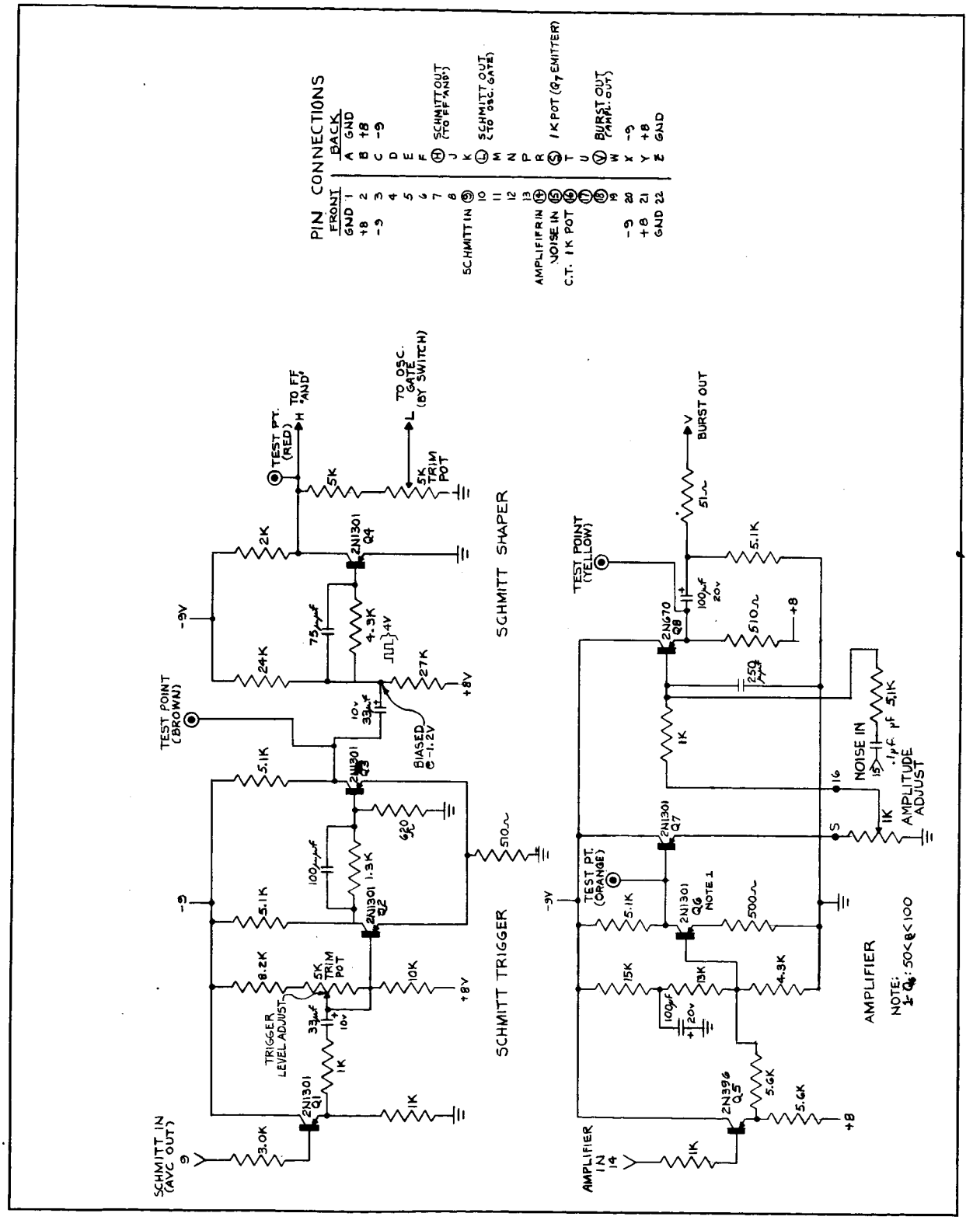
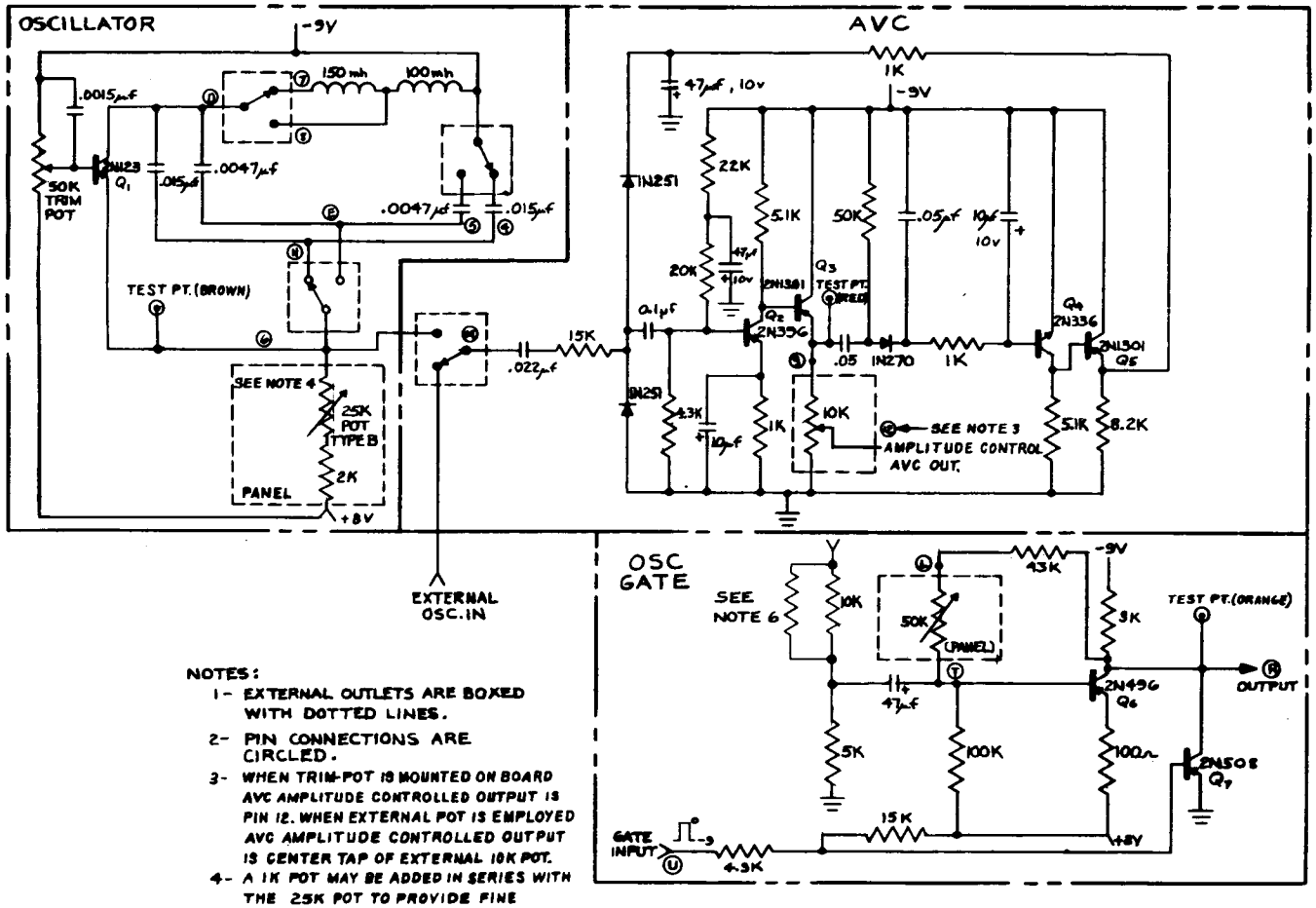


Figure 11 – Schmitt Trigger and Amplifier



NOTES:

1- EXTERNAL OUTLETS ARE BOXED WITH DOTTED LINES.

2- PIN CONNECTIONS ARE CIRCLED.

3- WHEN TRIM-POT IS MOUNTED ON BOARD AVC AMPLITUDE CONTROLLED OUTPUT IS PIN 12. WHEN EXTERNAL POT IS EMPLOYED AVC AMPLITUDE CONTROLLED OUTPUT IS CENTER TAP OF EXTERNAL 10K POT.

4- A 1K POT MAY BE ADDED IN SERIES WITH THE 25K POT TO PROVIDE FINE FREQUENCY ADJUSTMENT.

5- Q6: $10 < \beta < 30$

6- RESISTOR ADDED IN PARALLEL TO ATTENUATE OUTPUT SIGNAL SUCH THAT ALL OSCILLATOR GATES HAVE APPROX. SAME AMPLITUDE OUT.

(SEE NOTES 1 & 2)
PIN CONNECTIONS

FRONT		BACK
GND	1	A GND
+8	2	B +8
-9	3	C -9
	4	D
	5	E
	6	F
	7	H
	8	J
	9	K
	10	L
	11	M EXTERNAL (SCAN)
SEE NOTE 3	12	N
	13	P
	14	R
	15	S
	16	T
	17	U GATE INPUT
	18	V
CW	19	W
-9	20	X -9
+8	21	Y +8
GND	22	Z GND

Figure 12 – Oscillator, AVC, and Oscillator Gate Circuits

of the output. The reduced output is used to drive the oscillator gate (Figure 12) whenever square waves are desired.

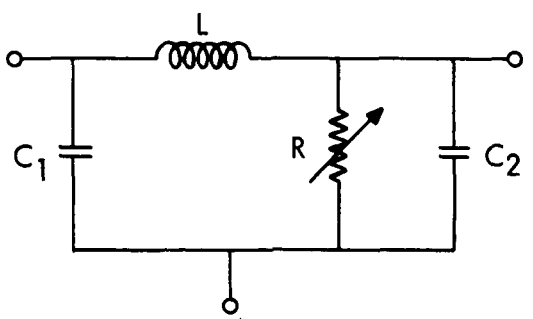
The input to the amplifier is an emitter-follower Q5 for high-input impedance, which drives an ac amplifier Q6 whose output is approximately 4.4vpp. The output amplitude is adjusted by an external front-panel potentiometer in the emitter of Q7; the output may be resistive mixed with noise and the combination of signal and noise is used to drive the emitter-follower at Q8. The series 51-ohm resistor protects the circuit against shorting of the output.

OSCILLATOR CIRCUIT

The first circuit is a continuously variable sinusoidal oscillator of the Colpitts type which, through external switch control, has the two frequency ranges of 4.5 to 15 kc and 15 to 45 kc. Each range is obtained by switching a separate LC network into the oscillator. The approximate center frequency of the oscillator for each tank is given by:

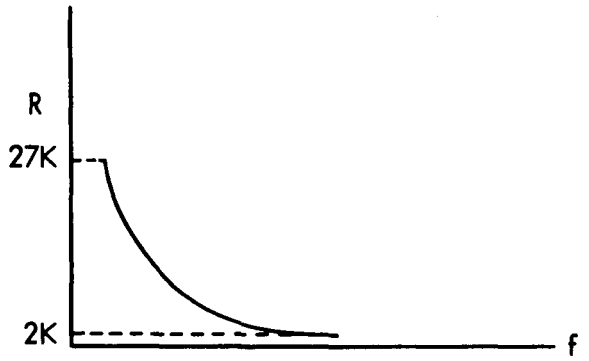
$$f = \frac{1}{2\pi\sqrt{LC_\tau}} \text{ where } C_\tau = \frac{C_1 C_2}{C_1 + C_2}$$

By adding a variable resistance (R) between the emitter and ac ground, the equivalent ac tank circuit appears as shown below:

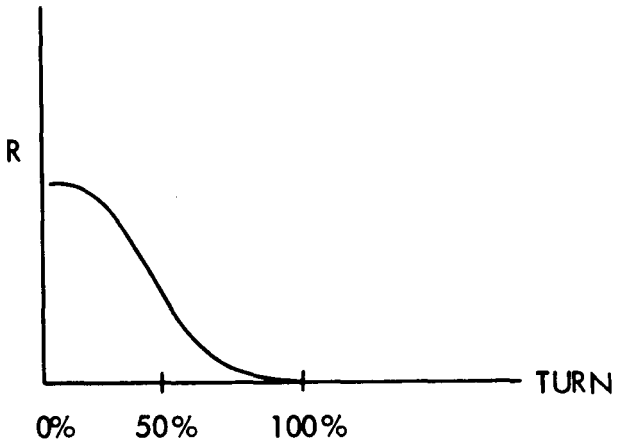


By varying R, the equivalent reactance provided by C_2 is altered and the center frequency of the network is changed. In the Mode II simulator, R is

the sum of a 25-kilohm potentiometer and a fixed resistor of 2 kilohms. The oscillator frequency variation with R is shown below:



Because the frequency varies nearly hyperbolically with R, a type-B logarithmic potentiometer having a curve as shown below is employed to provide an approximately linear variation of frequency with the turning of the frequency control.



AUTOMATIC VOLTAGE-CONTROLLED (AVC) CIRCUIT

The function of the second circuit is to automatically voltage-control either the internally generated frequency signal or an externally applied frequency signal so that the input to the oscillator gate will always be a constant-level signal.

The principle employed is in essence that of controlling the gain of a Class A amplifier through interrogation of the output signal level as shown in Figure 13.

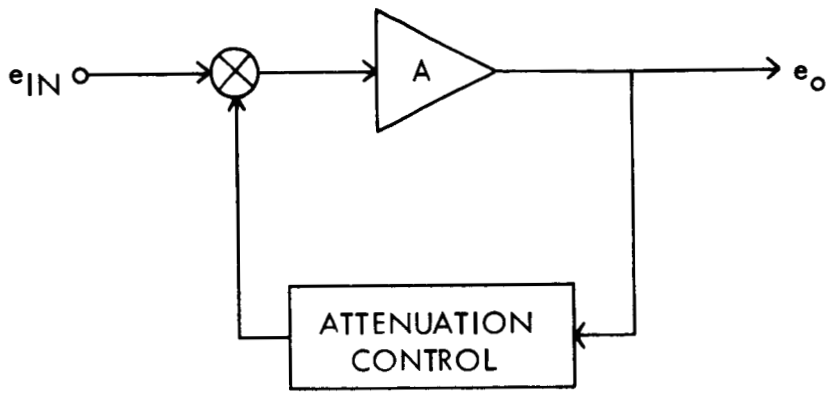


Figure 13 – AVC Loop

This is done by equivalently varying the shunt resistance of an L pad preceding the input to the Class A amplifier with a dc current that is a function of the output signal level of the amplifier. The L pad consists of a series resistor and an equivalent ac shunt resistance of two diodes which are dc biased in a region where, for changes in the dc current through the diode, the small signal diode resistance can be varied. Figures 14, 15, and 16 show the complete L pad, the ac equivalent, and the equivalent configuration seen by the input signal.

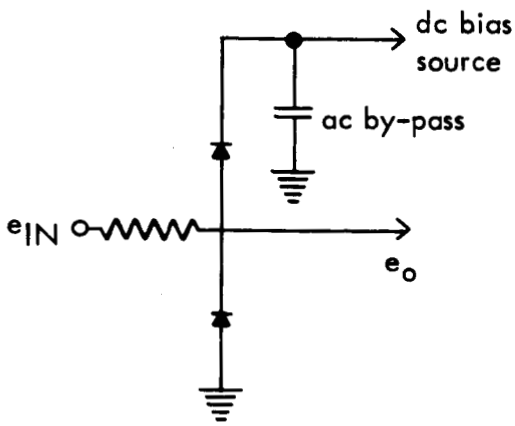


Figure 14 – Complete L Pad

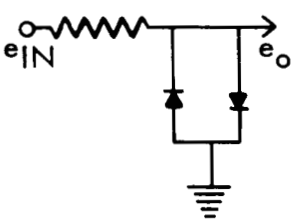


Figure 15 – AC-Equivalent L Pad

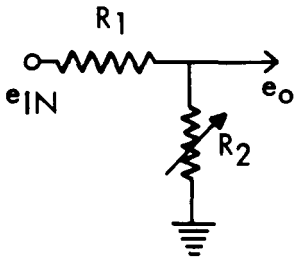


Figure 16 – Equivalent L Pad Seen by Input Signal

The variation of the small signal resistance with the dc bias current can be seen by reviewing the characteristic curve of the diode as shown in Figure 17, where V is chosen to be the ordinate and I the abscissa.

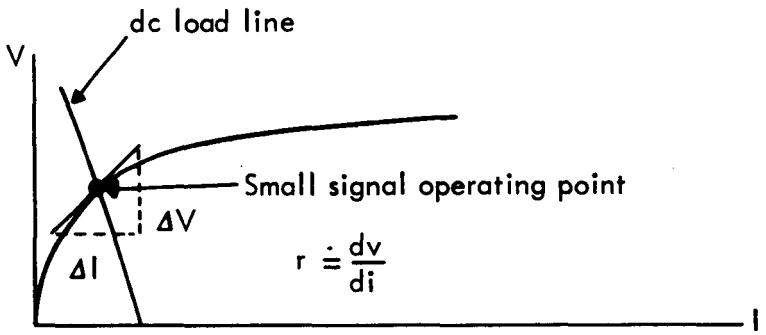


Figure 17 – Diode Characteristic Curve

The resistance exhibited by the diode is the tangent to the curve at the intersection of the dc bias current and the characteristic curve. For very small time-varying signals, the ac resistance is appreciably linear for a fixed dc operating point. By changing the quiescent operating point, the ac resistance is changed as shown.

The small variation from linearity is improved by using two diodes in parallel, one in an ac forward biased direction and one in a negatively biased direction; the ac resistance is then the parallel resistance of the two small signal resistances given by the two operating points of both diodes.

The dc bias current to the L pad is supplied by detecting and low pass-filtering the output of the Class A amplifier (Q_2) amplifying this voltage, and then providing a current as a function of this voltage.

OSCILLATOR GATE

The oscillator gate (Figure 12) digitally controls passage or infinite attenuation of a time-varying signal so that the signal dc level during the time of infinite attention is the dc center of the peak-to-peak levels of the signal during passage. This is done by biasing a Class A amplifier (Q_6) so that the output quiescent operating level is ground. Application of a symmetrical input signal will then vary about ground at the output of the amplifier. A saturating transistor (Q_7) is digitally controlled (at pin U) to turn this transistor full-on or full-off which infinitely attentuates the output of the Q_6 or fully passes the output of Q_6, respectively. The 2N508 was chosen for Q_7 because it has an extremely low saturating voltage.

The dc level of the output of Q_6 is externally controlled by varying a 50-k potentiometer in the bias network as shown in Figure 12.

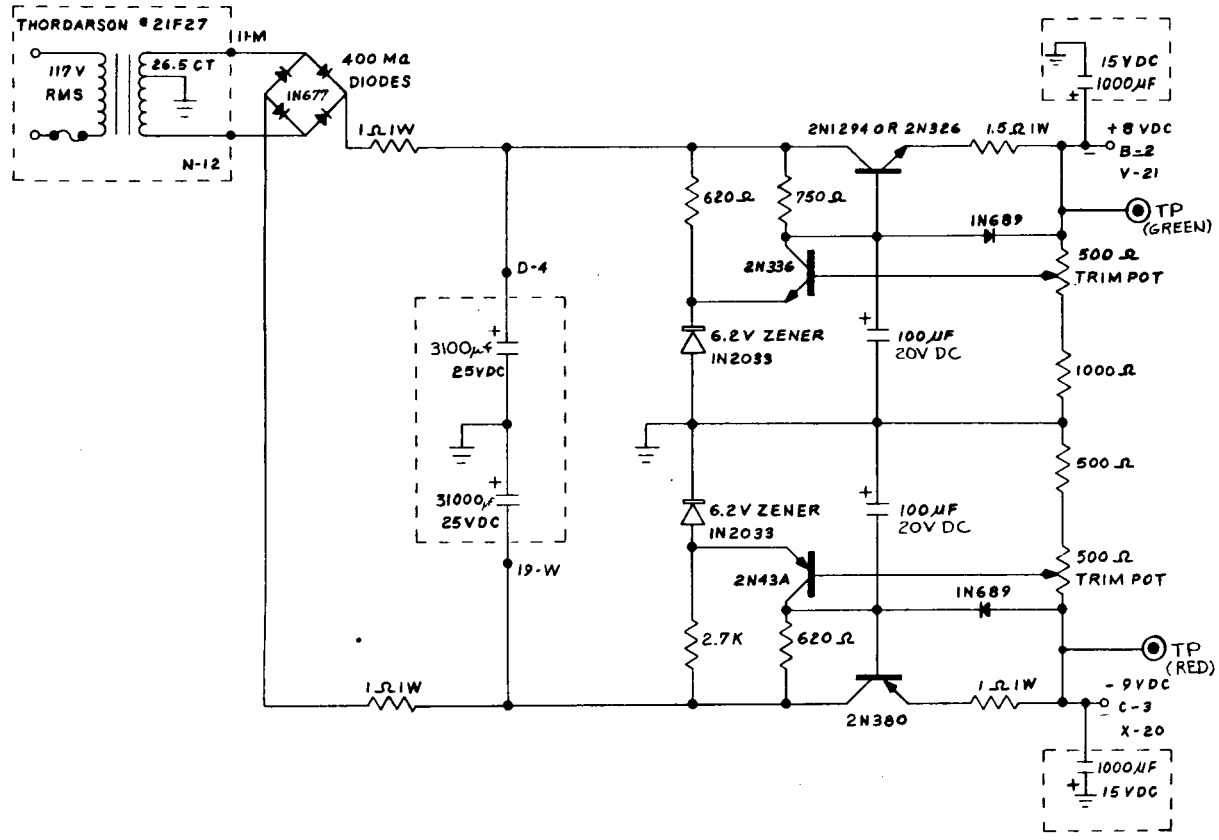
POWER SUPPLY

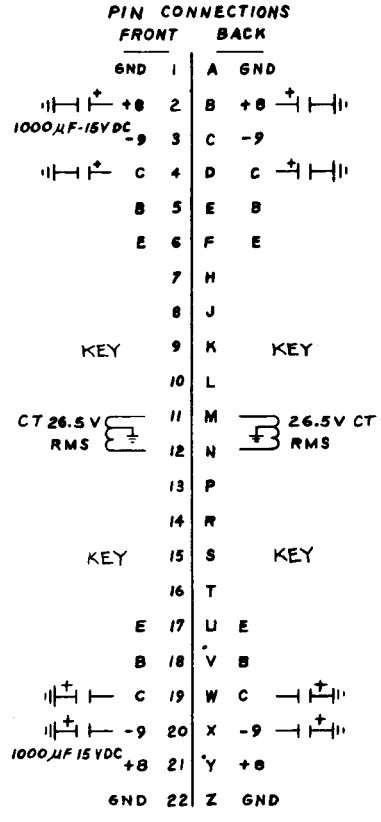
The power supply (Figure 18) consists of two voltage regulators, one for +8vdc and one for -9vdc. The +8vdc power supply will deliver 300 ma and the -9vdc supply will deliver 400 ma. Both regulators are of the series type in which regulation is made through control of a series power transistor by referencing the output of each supply through a divider network to a constant voltage source provided by a zener diode. Correction is made by varying the gain of the series power transistor through an amplifying stage with the infinite tesimal voltage differences seen between the zener diode and the divider network. Both regulators share the same transformer input through a full wave rectifier; each supply is filtered separately.

Each supply is protected against short circuits or excessive loads through current limiting. The supply voltages may be finely varied by adjusting the trimpots incorporated in the divider network of each regulator.

PERFORMANCE CHECK

This section describes the procedure for checking the simulator and setting all internal controls for proper operation.





NOTES:

1- EXTERNAL COMPONENTS ARE ENCLOSED WITH DOTTED LINES

2- LIMITING CURRENT WHEN OUTPUT IS SHORTED TO GND:
   -9 SUPPLY → 500 ± 40 MA (REGULATION TO 400 ± 50 MA)
   +8 SUPPLY → 300 ± 50 MA (REGULATION TO 250 ± 50 MA)

3- CIRCUIT BOARD HAS A BLACK LIFTER.

Figure 18 – Power Supply

All wave shapes and voltage levels should be made with front-panel switches in following positions (unless otherwise specified):

- All NAR/WIDE switches — wide position
- FREQ RANGE — high position
- SINEWAVE/SQ WAVE — SINEWAVE position
- INT OSC/EXT OSC switch — internal position
- BURST AMPLITUDE — maximum clockwise
- BURST DC LEVEL — maximum clockwise

All other controls will be used to obtain correct wave shapes. The printed circuit boards are numbered 1 to 6 from front to back.

Test equipment to be used includes: Tektronix 535 -A oscilloscope with dual trace amplifier, Simpson meter, and Hewlett-Packard oscillator.

1. Apply ac with power ON switch. Measure the dc voltages, -9 and +8, at test points on power-supply card (card 6). Green test point is +8; left trimpot adjusts this voltage. Red test point is -9; right trimpot adjusts this voltage.

2. Observing sawtooth wave at brown test point on card 3 (rundown), adjust this sawtooth with front-panel 50K pot, BURST-BLANK PERIOD, for a 20-millisecond sawtooth (Figure 19). Scope settings: Sweep time, 5 milliseconds/cm; vertical deflection, 2 volts/cm; sync, internal negative.

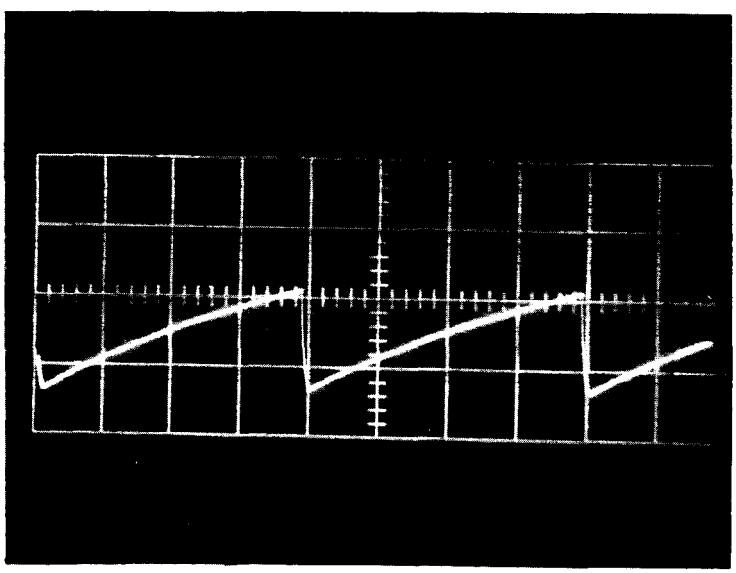


Figure 19 – Brown Test Point, Card 3

3. Observing sawtooth wave at red test point on card 3 (rundown), adjust this sawtooth with front-panel control BURST WIDTH for a 10-millisecond blank (Figure 20). Scope settings: Sweep time, 5 milliseconds/cm; vertical deflection, 2 volts/cm; sync, internal negative.

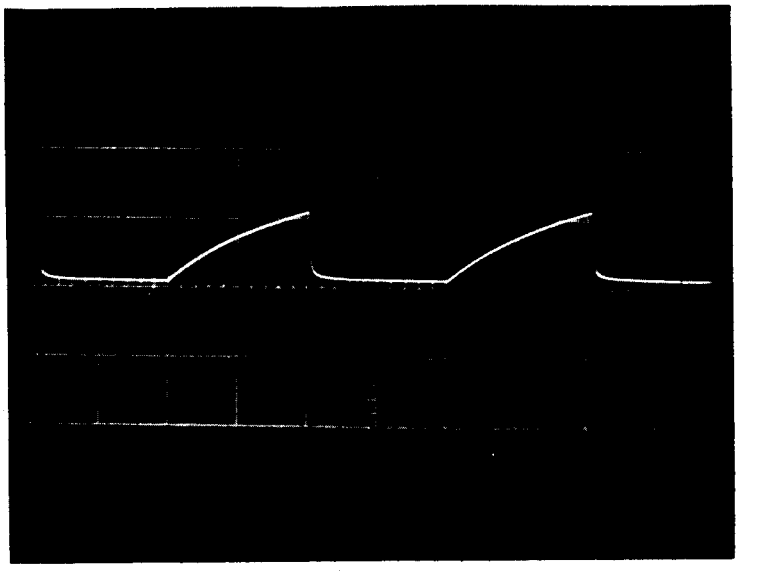


Figure 20 – Red Test Point, Card 3

4. Observing sawtooth waves at red and brown test points on card 3 (rundown), the time relationship should be: During the time of the 20-millisecond sawtooth there should appear a 10-millisecond sawtooth and a 10-millisecond blank (Figure 21). Scope settings: Sweep time, 5 milliseconds/cm; vertical deflection, 2 volts/cm; sync, internal negative

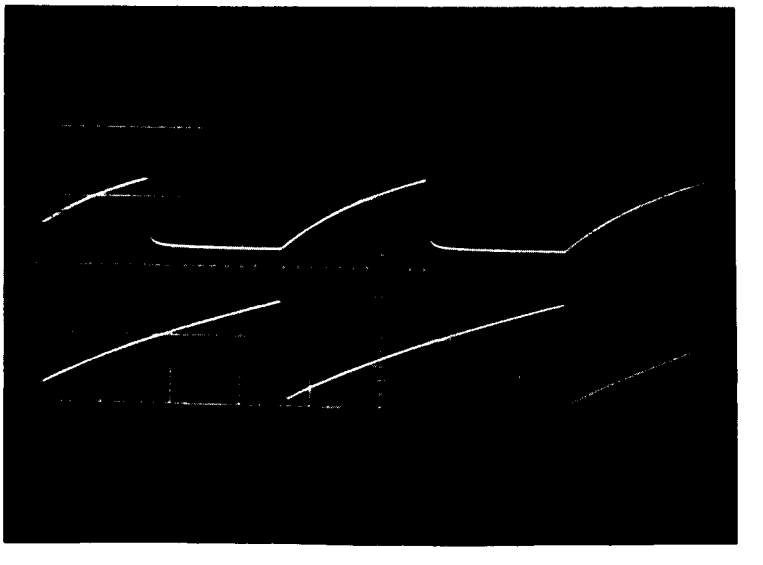


Figure 21 – Red and Brown Test Points, Card 3

5. Observing sawtooth wave at yellow test point, card 3 (rundown), adjust this sawtooth for a minimum of 5 milliseconds with SYNC BURST POSITION control on front panel. This wave shape is obtained by using external sync from burst 15 connector. Scope settings remain the same as for last check.

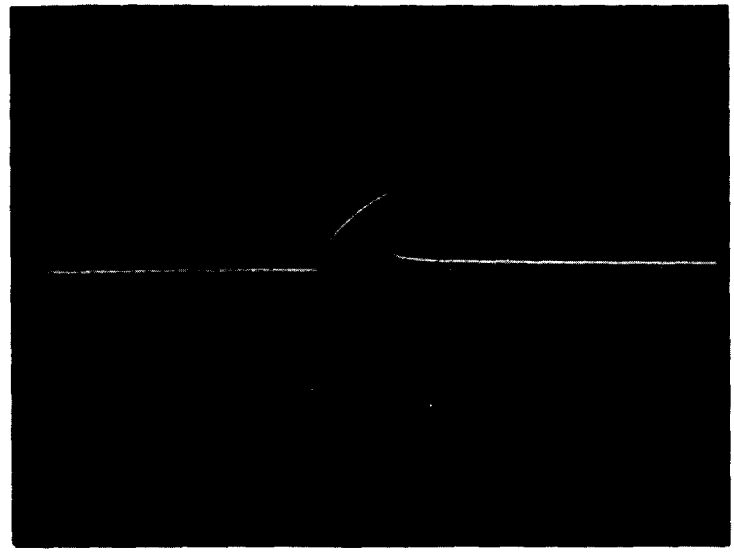


Figure 22 – Yellow Test Point, Card 3

6. Observing wave shape at orange test point, card 3 (rundown), adjust sawtooth wave for 10 milliseconds with front-panel control SYNC BURST WIDTH. Obtain external sync from burst 15 connector on front panel.

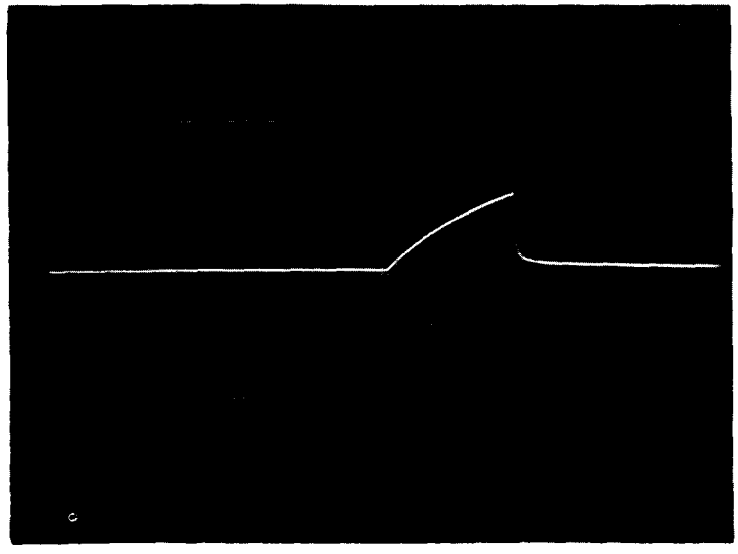


Figure 23 – Orange Test Point, Card 3

7. Observe wave shapes at orange and yellow test points on card 3 (rundown) and check to determine if the negative-going edge of the SYNC BURST POSITION sawtooth (which is 5 milliseconds in duration) occurs at the beginning of the 10-millisecond sawtooth (Figure 24). Scope settings: Sweep time, 5 milliseconds/cm; vertical deflection, 2 volts/cm; sync, external from burst 15 connector.

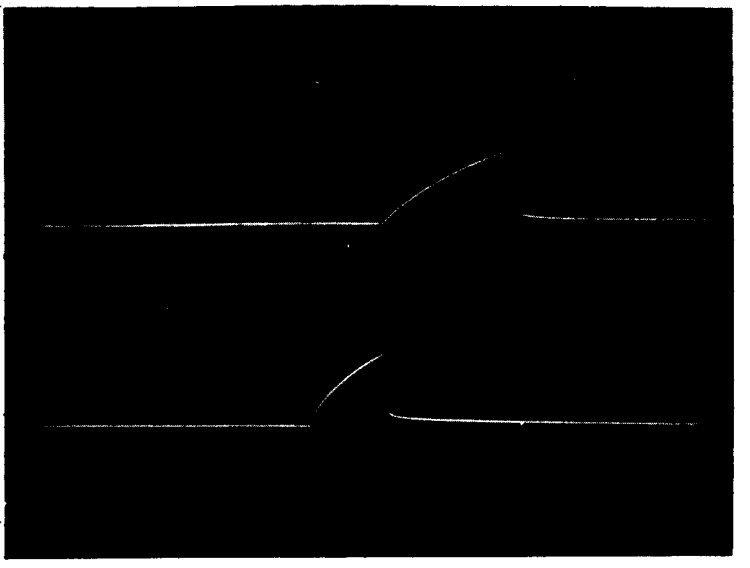


Figure 24 – Orange and Yellow Test Points, Card 3

8. Obtain a symmetrical waveform at brown test point, card 2 (oscillator gate). Set OSC FINE control to midrange by adjusting OSC COARSE control on front panel, simultaneously adjusting left trimpot on card 2 until no noticeable change occurs in the bias set and the peaking of the oscillator. This condition gives equal swing above and below ground (Figure 25). Scope settings: Sweep time, 20 milliseconds/cm; vertical deflection, 2 volts/cm; sync, internal positive.

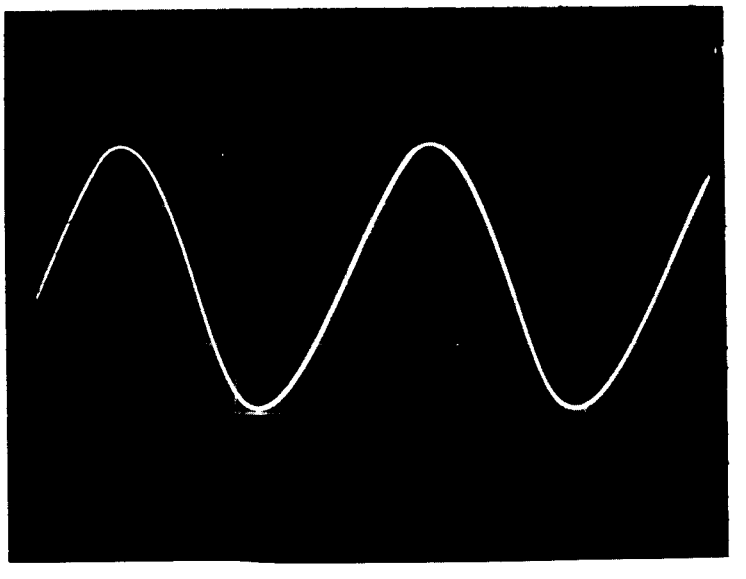


Figure 25 – Brown Test Point, Card 2

9. Observe square wave at brown test point, card 1 (Schmitt and amplifier). Obtain a symmetrical waveform by adjusting left trimpot on card 1 (Figure 26). Scope settings: Sweep time, 20 milliseconds/cm; vertical deflection, 2 volts/cm; sync, internal negative.

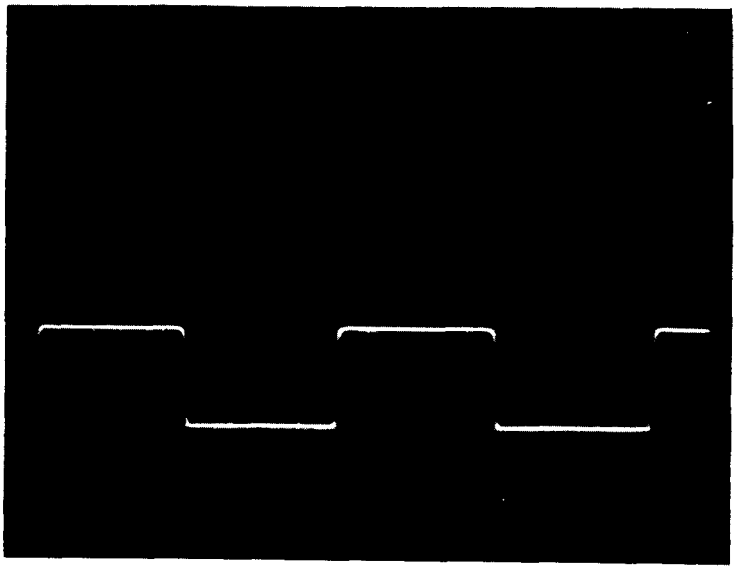


Figure 26 – Brown Test Point, Card 1

10. Adjust sinewave at burst OUT connector on front panel for maximum amplitude with right trimpot on card 2 (oscillator gate) before saturation occurs at about 4 volts. (Note: This will not give best sinewave operation; see Figure 27.) Scope settings: Sweep time, 0.1 millisec/cm; vertical deflection, 2 volts/cm; sync, internal negative.

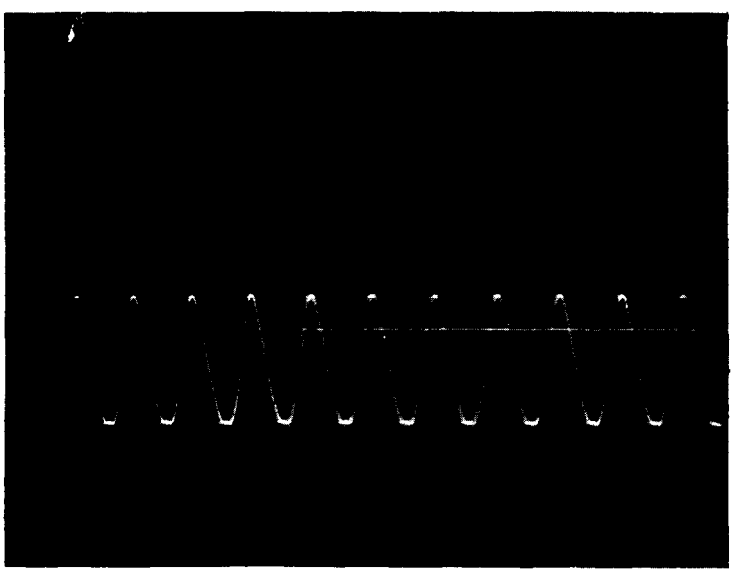


Figure 27 – Sinewave Adjustment

11. While monitoring BURST OUT, move SINEWAVE/SQ WAVE switch to SQ WAVE position. Adjust SQ WAVE for best symmetrical wave above and below ground with trimpot on right of card 1 (Schmitt and amplifier); approximate 6-1/2 volts peak-to-peak. When this is complete, throw switch back to SINEWAVE position. Scope settings: Sweep time, 0.1 milliseconds/cm; vertical deflection, 2 volts/cm.

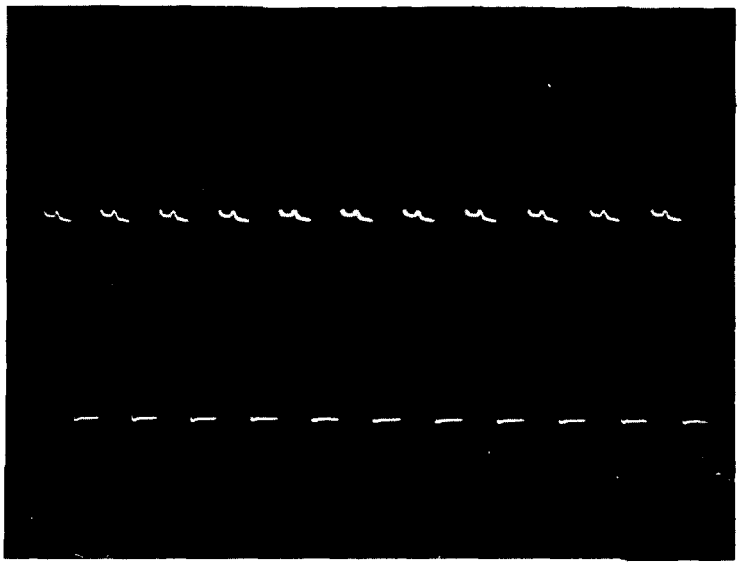
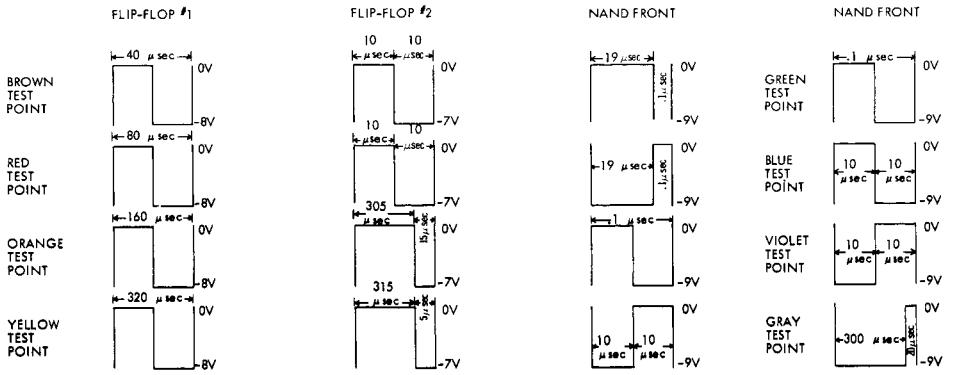
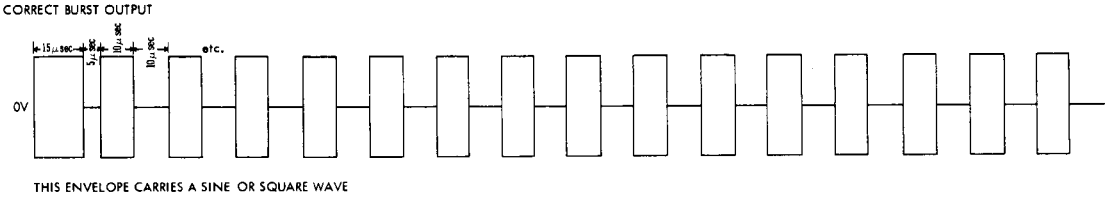


Figure 28 – Square Wave Adjustment

12. At this point check wave shapes and voltage levels as shown in Figure 29.

13. Now observe BURST OUT as compared to SYNC BURST POSITION, yellow test point. Obtain scope sync from burst 15 connector on front panel. If all adjustments are correct, the result will look like Figure 30. Note that, by increasing the SYNC BURST POSITION by 15 milliseconds, sync burst has moved to burst 1 as seen in Figure 31.





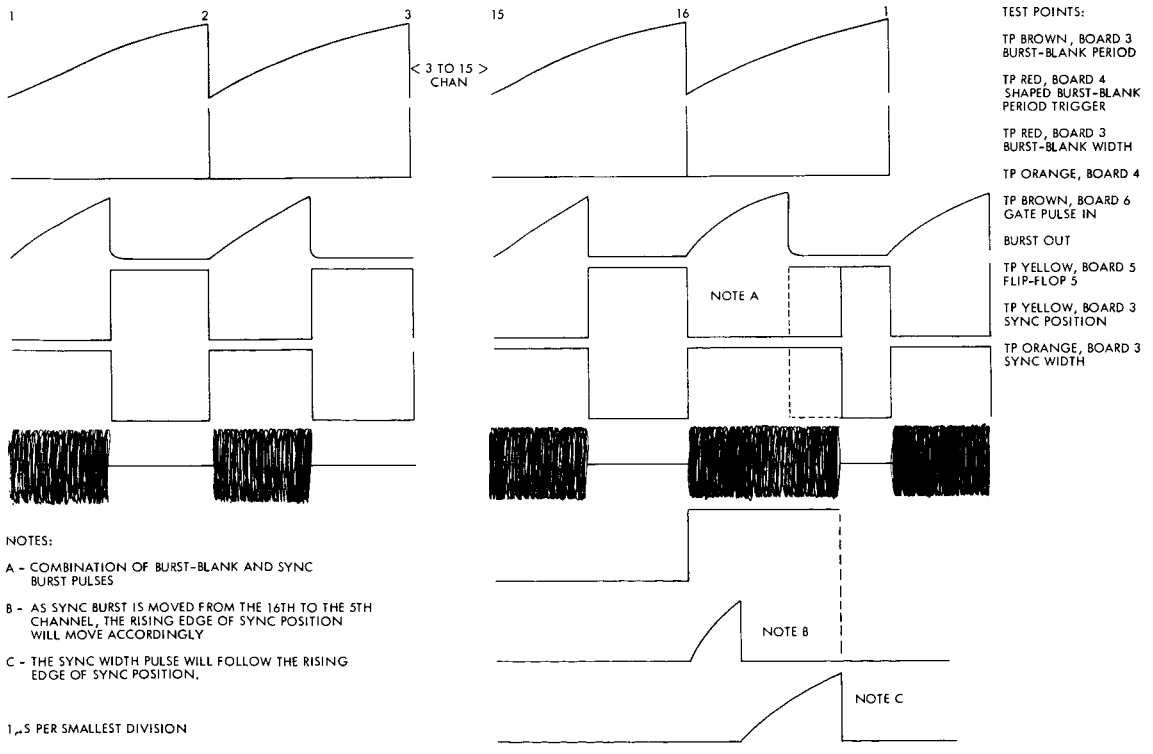


Figure 29 – Typical Waveforms

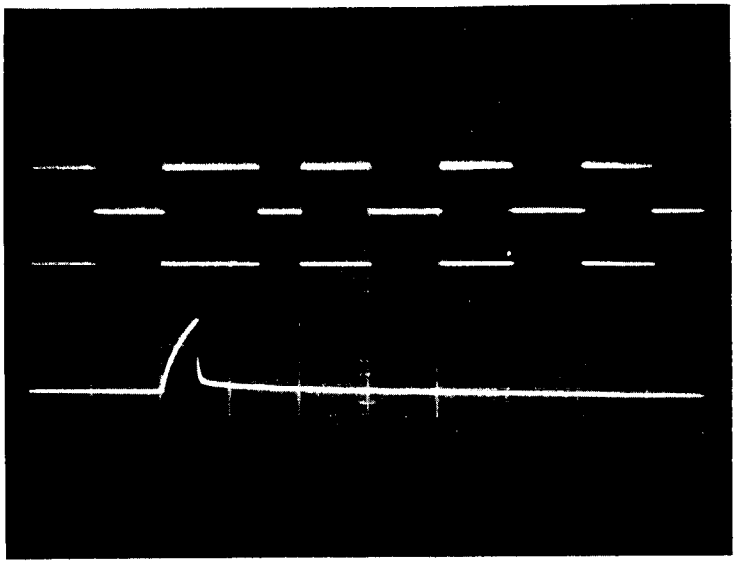


Figure 30 – Oscilloscope Pattern Showing Correct Adjustment

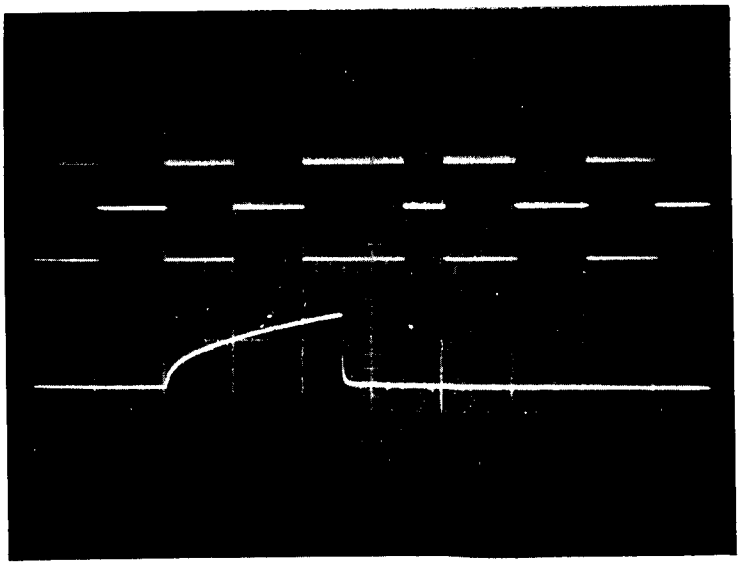


Figure 31 – SYNC BURST Variation